12.3 A 72mW 0.03mm² Inductorless 40Gb/s CDR in 65nm SOI CMOS

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CMOS is rapidly becoming an interesting option for data links at 40Gb/s [1]. In this paper, the key techniques in designing a CDR circuit are discussed. First, the use of a phase-programmable PLL [2] architecture allows implementing a dual-loop CDR architecture [3] without the need for costly phase rotators. Second, most analog circuits in the CDR use static-CMOS design style that allows operating the transistors with high gate overdrive while occupying a small area. In addition, using static-CMOS style in the VCO provides the required large signal swings and fast fall times for the pass transistors in the sampling stage.

Central part of the dual-loop [3] quarter-rate CDR circuit, shown in Fig. 12.3.1, is the phase-programmable PLL that generates 16 clock phases. The PLL consists of a ring VCO, a phase-detector array, a loop filter, and a V/I converter. All phases of the PLL can be simultaneously shifted by some digital value [2]. This is achieved by summing the individual XOR phase-detector outputs, weighted by digitally programmable factors α_n. At each point in time, 2 phase detectors locking to 2 adjacent phase octants are active. By controlling the relative weights of the phase-detector outputs, α_n and α_{n+1}, a fine adjustment of the phase between the 2 clock octants is achieved.

The α_n values are set by controlling the currents in the phase detectors with an integrated DAC. To achieve the required phase resolution, the DAC consists of 8 thermometer-coded bits plus 2 binary-coded bits, generating a total of 35 fine steps between 2 octants. This results in 280 steps for a 100ps reference clock period, or 70 steps for a UI of 25ps. By using a phase-programmable PLL approach, phase rotators, conventionally used in dual-loop CDR architecture, can be avoided and the clock path is minimized.

The PLL is locked to the 10GHz reference clock with >1GHz bandwidth, which to a high degree suppresses VCO noise. The 8 even VCO phases, $\phi_{2n,}$ enter the phase-detector array. The 8 odd phases, ϕ_{2n+1}, are used in the high-speed sampling stage that creates 4 data $d_{0\text{-}3}$, and 4 edge samples, $e_{0\text{-}3,}$ in every clock cycle. The sampling stage is followed by a 4:8 DEMUX, generating 8 data and 8 edge samples at a rate of 5GHz. The data bits are fed to an integrated PRBS 15 checker, generating an error signal when any of the 8 data bits is incorrectly received, which is then sent to the chip output.

The phase tracking loop is implemented by a digital DLL. The early/late-signal-generation logic generates a single *early* or *late* signal from the 8 data bits, $d_{0\text{-}7}$, and 8 edge bits, $e_{0\text{-}7}$, by a 2-step majority vote, which is then accumulated in the digital loop filter. A phase step (*up* or *down*) is induced when the overhang of *early* or *late* signals is greater than 4. The phase position is then encoded in the digital control bits to set the α-DAC values of the phase-detector array that closes the CDR loop.

The VCO, displayed in Fig. 12.3.2, consists of 8 inverter stages. The VCO is based on a regulated ground approach [2], where an opamp regulates the ground potential V_{creg} in order to match the loop filter voltage V_c. Regulating the ground node is preferred to regulating V_{DD} since all input signals are referenced to V_{DD}, and small NFETs can be used in the regulating current source for the VCO and the XOR phase-detector cells.

The delay of the VCO stages can be digitally adjusted, which serves 2 purposes: First, it allows maximizing the swing in the VCO for different process corners. Second, it allows adjusting the timing between *data* and *edge* samples to account for the fact that for a given channel the maximum vertical eye opening is not necessarily in the middle of the data eye. The delay stages are therefore divided into 2 groups, labeled A and B, which receive separate control values for the delay setting, *offsA* and *offsB*. Figure 12.3.3 shows the simulated timing between the data and the edge samples as a function of the programmed value. Note that the *even* phases, ϕ_{2n}, going into the phase detector always stay equidistantly spaced, since there is always a fast (e.g. A) delay cell followed by a slow (e.g. B) delay cell between 2 adjacent clock phases.

Figure 12.3.4 displays the data-sampling stage. To achieve high-speed operation, the sampler consists of a T/H stage, implemented as NMOS pass transistors T_1, T_{1b}, followed by a sense-amp latch. FETs, operated as switches, achieve very high time resolution, provided that the input-clock fall times are sufficiently short, and the clock swing is high enough for the expected signal swing. The VCO clock, ϕ_{2n+1}, is therefore fed to a high slew-rate inverter, running from the regulated VCO supply, V_{creg}, that sharpens the edge at its output. Since the common-mode voltage of the input data $V_{in,cm} = (V_{in}+V_{inb})/2$, and the following latch is V_{DD}-0.3V, the common mode of the sampling clock at the gates of T_1, T_{1b} is raised to an externally supplied voltage $V_{\phi,cm}$ (set to V_{DD}) via a high valued resistance R_{cm} and coupling capacitance C_c. A worst-case clock swing of 0.9V with <8ps fall transition time is achieved.

A full-swing converter (FSC in Fig. 12.3.4) converts the clock from the regulated supply domain of the VCO to the unregulated full-swing V_{DD} domain of the following sense-amp latches. Since the actual sampling time is defined by the preceding hold stage, delay variations in the FSC due to power-supply noise do not influence jitter tolerance.

The CDR circuit is fabricated in a 65nm digital CMOS SOI technology. The loop filter logic, the PRBS checker, and the output MUX logic are synthesized into one block of static CMOS logic. The test circuit also contains a shift register to provide digital control values, and 2 inverter-based output buffers to monitor the error signal of the PRBS15 checker, a divided-by-2 clock signal, and the data samples.

A differential input signal from a BiCMOS 4:1 MUX [4] and Anritsu 1775A parallel signal generator is provided to the RX, of which the single-ended input eye is shown in Fig. 12.3.5(a). Error-free operation (BER<10^{-12}) is measured at 40Gb/s with a PRBS15 data sequence and a maximum frequency offset of ±400ppm. The internal eye opening is measured by turning off the phase-tracking logic and sweeping the delay of the input data externally, resulting in an error-free region of 11ps.

A jitter tolerance measurement, shown in Fig. 12.3.5(b), is performed at a maximum data rate of 27Gb/s due to a limitation of the measurement equipment. The measurement is repeated with a small frequency offset of 1ppm to cover all phase positions. The CDR circuit consumes 75mW from a 1.2V supply at 40Gb/s, with 3mW consumed by the PRBS checker; this results in a power efficiency for the proposed CDR+1:8 DEMUX of 1.8mW/Gb/s. Figure 12.3.6 shows a comparison with prior work [1, 5, 6, 7]. The layout and a die micrograph of the receiver circuit that ocuupies 190×150µm² are shown in Fig. 12.3.7.

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References:
[1] J. Lee, B. Razavi, "A 40-Gb/s Clock and Data Recovery Circuit in 0.18-µm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2181 - 2190, Dec., 2003.
[2] T. Toifl, C. Menolfi, P. Buchmann, et al., "0.94ps-rms-Jitter 0.016mm² 2.5GHz Multi-Phase Generator PLL with 360° Digitally Programmable Phase Shift for 10Gb/s Serial Links," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2700–2712, Dec., 2005.
[3] S. Sidiropoulos, M. Horowitz, "A Semi-Digital Dual Delay-Locked Loop," *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1683-1692, Nov., 1997.
[4] M. Meghelli, A.V. Rylyakov, S.J. Zier, et al., "A 0.18µm SiGe BiCMOS Receiver and Transmitter Chipset for SONET OC-768 Transmission Systems," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2147-2154, Dec., 2003.
[5] B. Casper, J. Jaussi, F. Oapos Mahony, et al., "A 20Gb/s Forwarded Clock Transceiver in 90nm CMOS," *ISSCC Dig. Tech Papers*, pp. 90-91, Feb., 2006.
[6] C. Kromer, G. Sialm, C. Menofli, el al., "A 25Gb/s CDR in 90nm CMOS for High-Density Interconnects," *ISSCC Dig. Tech Papers*, pp. 326-327, Feb., 2006.
[7] D. Kucharski, Kornegay, K.T., "2.5 V 43-45 Gb/s CDR Circuit and 55 Gb/s PRBS Generator in SiGe Using a Low-Voltage Logic Family," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2154 - 2165, Sept., 2006.

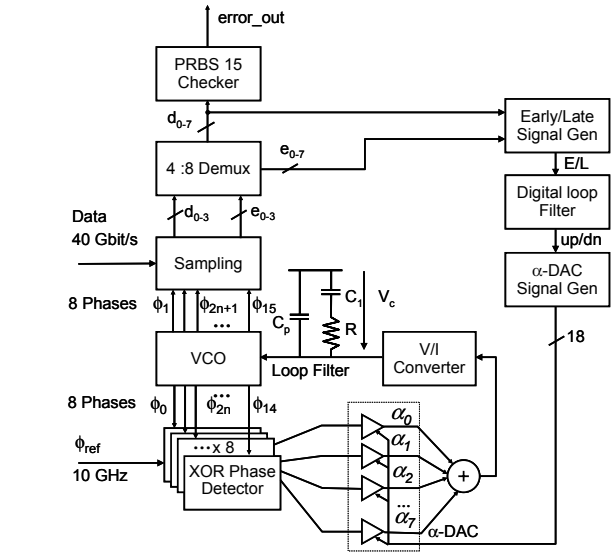


Figure 12.3.1: Block diagram of the CDR circuit.

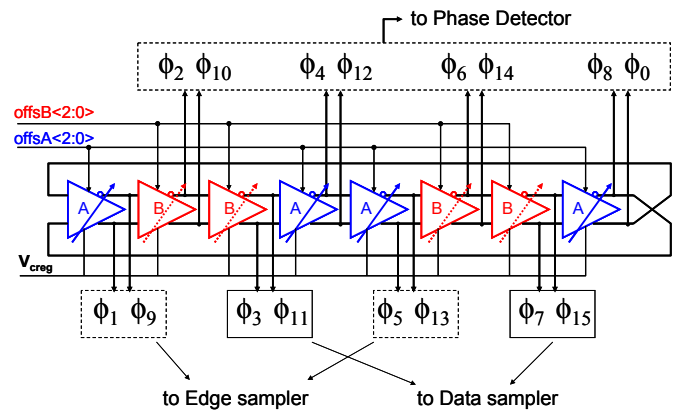


Figure 12.3.2: VCO block diagram.

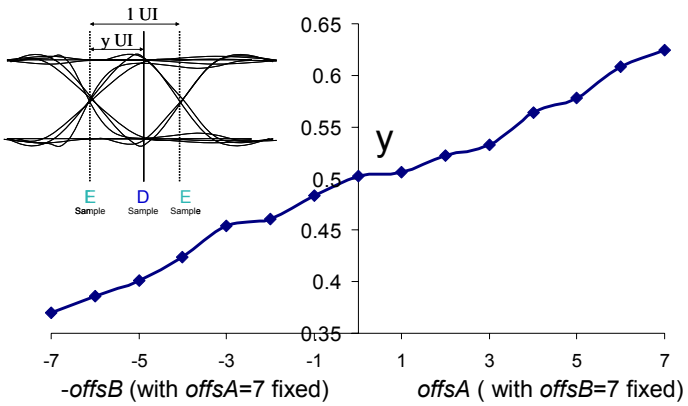


Figure 12.3.3: Data to Edge sample timing offset versus programmed value.

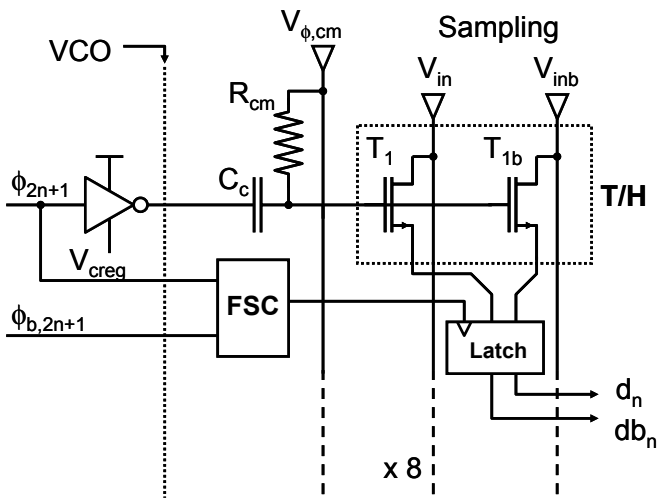
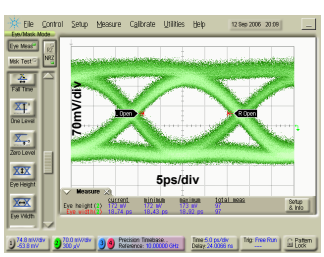
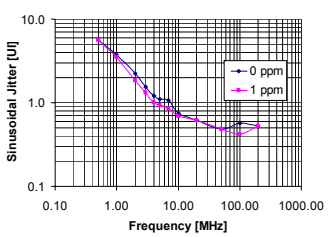


Figure 12.3.4: Schematic of high-speed sampling stage.



(a)

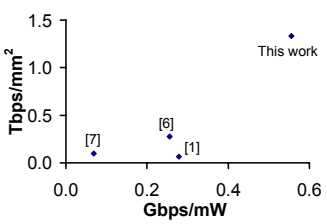
40Gb/s input eye diagram



(b)

Jitter tolerance @ 27Gb/s

Figure 12.3.5: 40Gb/s input eye and jitter tolerance at 27Gb/s.



	[1]	[5]	[6]	[7]	This work
Data rate	40Gb/s	20Gb/s	25Gb/s	45Gb/s	40Gb/s
Demux	1:4	NA	1:4	1:1	1:8
Power Diss.	144mW	NA	98mW	600mW	72mW
Area	0.64mm² (estim.)	0.07mm²	0.09mm²	0.47mm² (estim.)	0.03mm²
Gb/s/mW	0.28	NA	0.26	0.07	0.56
Tb/s/mm²	0.06	0.29	0.28	0.10	1.33
BER	10^{-6}	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$
Technology	0.18µm CMOS	90nm CMOS	90nm CMOS	120GHz SiGe	65nm CMOS SOI

Figure 12.3.6: High-speed CDR circuit comparison.

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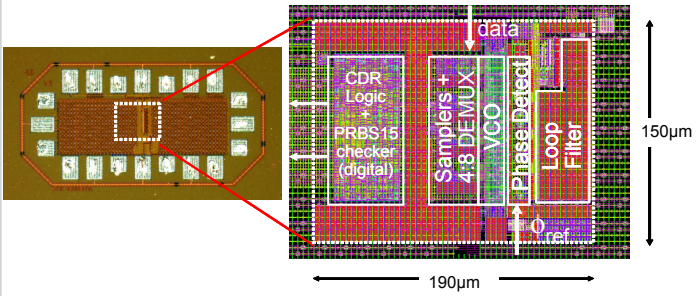

Figure 12.3.7: Chip micrograph and layout.

